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MOTOROLA

MC33410

Product Preview

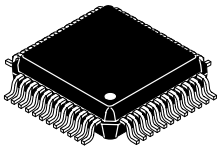
Dual CVSD/PLL Cordless Phone System

DUAL CVSD/PLL CORDLESS PHONE SYSTEM

SEMICONDUCTOR TECHNICAL DATA

The MC33410 Dual CVSD/Cordless Phone system is designed to fit the requirements of a 900 MHz digital cordless telephone system. The device contains a CVSD (Continuously Variable Slope Delta Modulator/Demodulator) Encoder to digitize the speech for the RF transmission, and a CVSD Decoder to reconstruct the received digital speech from the RF receiver. Provisions are made to transmit and receive data as well. Included are three PLLs (Phase–Locked Loops). Two are intended for use with external VCOs and 64/65 or 128/129 dual modulus prescalers, and can control the transmit and receive (LO1) frequencies for the 900 MHz communication. The third PLL is configured as the 2nd local oscillator (LO2), and is functional to 80 MHz. Also included are muting, audio gain adjust (internal and external), low battery/carrier detect, and a wide range for the PLL reference frequency. The power supply range is 2.7 to 5.5 V. A data only (non–voice) mode is also included.

- Two Complete CVSD Sections for Full Duplex Operation
- Two PLLs and an LO Suitable for a 900 MHz System
- Adjustable Detection for Low Battery or Carrier Signal (RSSI)
- Minimal External Components
- Encode Path Includes Adjustable Gain Amplifiers, Filters, Mute, CVSD Encoder, Data Insert, and Scrambler
- Decoder Path Contains Data Slicer, Clock Recovery, Descrambler, Data Detect, CVSD Decoder, Filters, Mute and Power Amplifier
- Data can be Transmitted During Voice Conversation with Minimal or No Noticeable Audio Disruption
- Idle Channel Noise Control
- Independent Power Amplifier with Differential Outputs, Mute
- Selectable Frequency for Switched Capacitor Filters, CVSD Function, PLLs, and the LO
- Reference Frequency Source can be a Crystal or System Clock
- Serial µP Port to Control Gain, Mute, Frequency Selection, Phase Detector Gain, Power Down Modes, Idle Channel Control, Scrambler Operation, Low Battery Detect, and Others
- Mode Available for Data Only Transmission (non–voice)
- Ambient Temperature Range: –40 to 85°C
- Power Supply Range: 2.7 to 5.5 V
- Power Down Modes for Power Conservation
- 48 Pin LQFP with 0.5 mm Lead Pitch



FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(LQFP–48)

ORDERING INFORMATION

Device	Operating Temperature	Package
XC33410FTA	–40° to +85°C	LQFP–48

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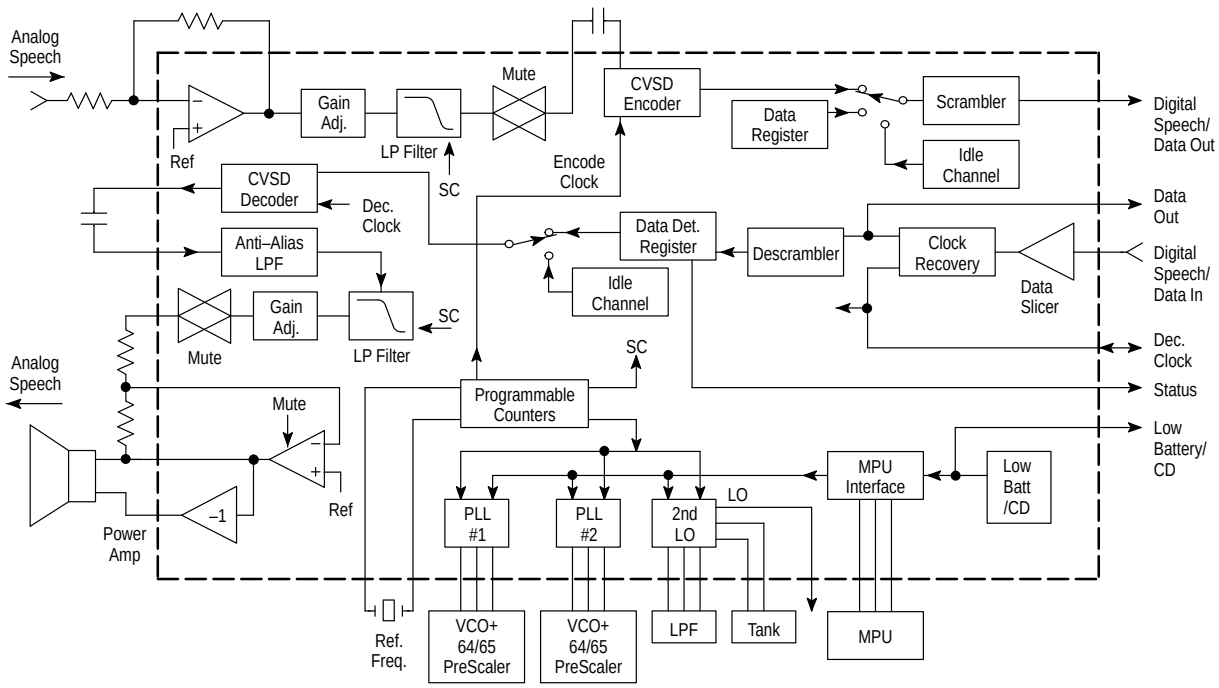
Simplified Block Diagram

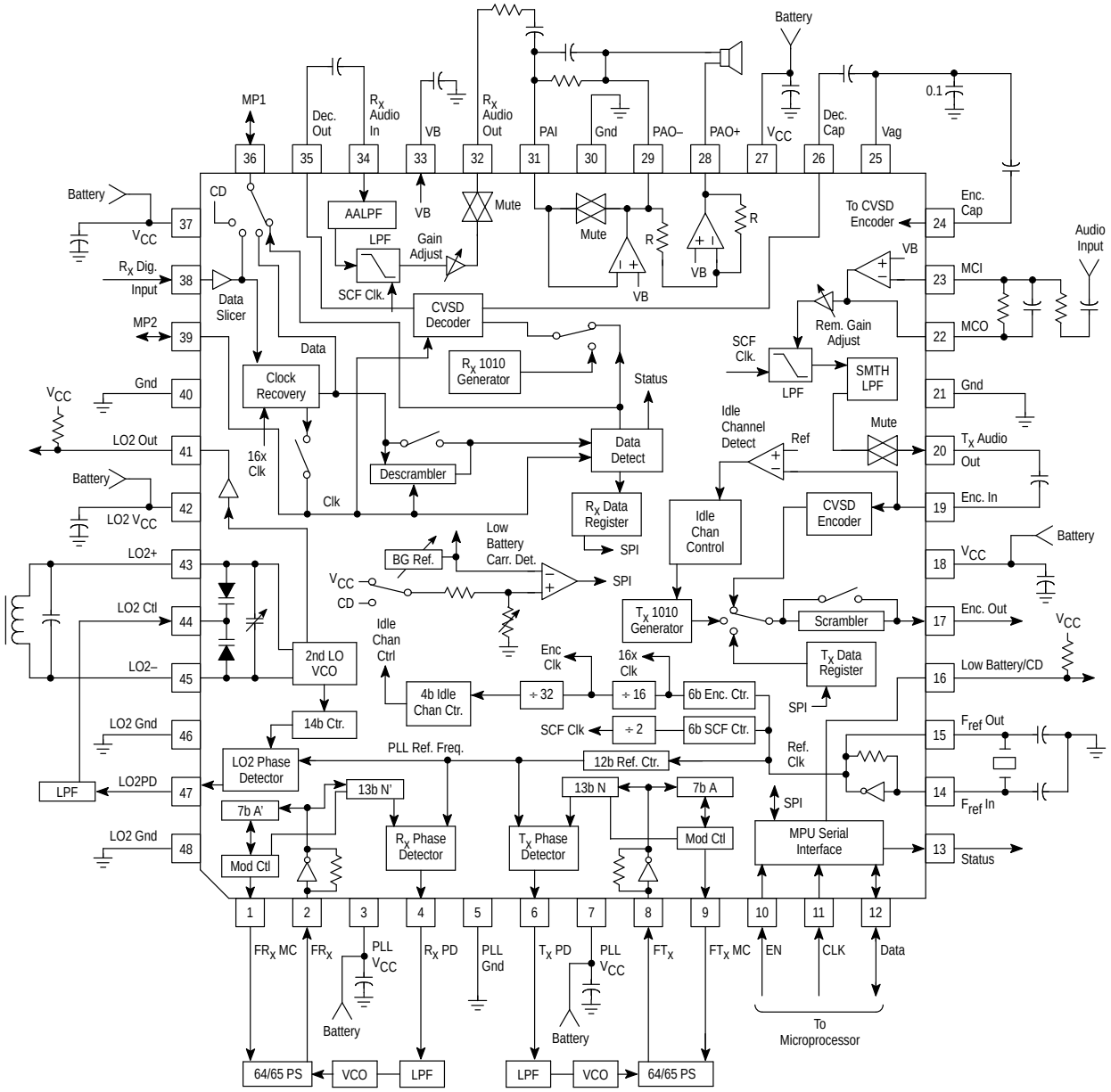


PRELIMINARY SPECIFICATIONS (Subject to change)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage		–	2.7 to 5.5	–	V
Supply Current (All sections active)		–	13	–	mA
Remote Gain Adjust Range		–	16	–	dB
Receive Path Gain Control Range		–	28.5	–	dB
Output Current Capability (PAO+, PAO–)		–	±5.0	–	mA
Max. 2nd LO frequency		–	80	–	MHz
Phase Detector Charge Pump Output Current High Low		 – –	 ±400 ±100	 – –	µA
Digital Input Signal Amplitude to Data Slicer		–	>200	–	mVpp
Operating Ambient Temperature		–	–40 to +85	–	°C

NOTE: 1. Above specs represent design objectives, and are subject to change.

Figure 1. Typical Applications Circuit



NOTE: Pin numbers are not firm and are not to be used for design–in purposes.

RECOMMENDED OPERATING CONDITIONS (Subject to change)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage		–	2.7 to 5.5	–	V
CVSD Clock Rate		–	32, 50, or 64	–	kHz
Encoder in Signal Level (max)		–	3.0	–	V_{pp}
Peak Output Current at PAO+, PAO–		–	±5.0	–	mA
Reference Frequency Amplitude (F_{ref} In)		–	>200	–	mVpp
R_X Digital Input Signal Amplitude Min Max		 – –	 0.20 0 to V_{CC}	 – –	V_{pp}
Crystal or Reference Frequency at Pin 14		–	4.0 to 18.25	–	MHz
Max. Input Frequency at FR_X, FT_X		–	TBD	–	MHz
LO2 VCO Control Voltage (Pin 44)		–	TBD	–	V
Max. 2nd LO Frequency		–	80	–	MHz
12 Bit Reference Counter Range (Note 1)		–	3 to 4095	–	–
13 Bit N Counter Range (Note 1)		–	3 to 8191	–	–
7 Bit A Counter Range (Note 1) with a 64/65 Modulus Prescaler with a 128/129 Modulus Prescaler		 – –	 0 to 63 0 to 127	 – –	–
14 Bit LO2 Counter Range (Note 1)		–	12 to 16383	–	–
6 Bit Counters (for SCF and Encode Clock) (Note 1)		–	3 to 63	–	–
Receive Path Gain Control Code Range (Note 1)		–	6 to 25	–	–
Operating Ambient Temperature		–	–40 to 85	–	°C

NOTES: 1. Values specified are pure numbers to the base 10.
2. Above specs represent design objectives, and are subject to change.

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	FR_X MC	Modulus Control Output to the R_X 64/65 or 128/129 dual modulus prescaler.
2	FR_X	Input to the R_X PLL.
3	PLL V_{CC}	Supply pin for the R_X PLL section. Allowable range is 2.7 to 5.5 V.
4	R_X PD	Phase detector charge pump output of the R_X PLL.
5	PLL Gnd	Ground pin for the PLL sections.
6	T_X PD	Phase detector charge pump output of the T_X PLL.
7	PLL V_{CC}	Supply pin for the T_X PLL section and the MPU Serial Interface section. Allowable range is 2.7 to 5.5 V.
8	FT_X	Input to the T_X PLL.
9	FT_X MC	Modulus Control Output to the T_X 64/65 or 128/129 dual modulus prescaler.
10	EN	Enable input for the µP port. This signal latches in the register address and data.
11	CLK	Clock input for the µP port. Maximum frequency is 2.0 MHz.
12	Data	Bi–directional data line for the µP port. In Data Modem mode, this pin provides the recovered clock.
13	Status	Logic output which indicates that a predetermined 16 or 24–bit code word has been detected in the Data Detect register, and the following data word has been loaded into register 10. In Data Modem mode, this pin provides the Transmit Data clock.
14, 15	F_{ref} In, F_{ref} Out	A crystal, in the range of 4.0 to 18.25 MHz can be connected to these pins to provide the reference frequency. If an external reference source is used, it is to be capacitively coupled to F_{ref} In.

NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Description
16	Low Battery/CD	An open collector output. When low, indicates either the supply voltage (V_{CC}) is low, or the carrier level is above the threshold. This output is off when disabled.
17	Enc Out	The digital output of the scrambler, which passes data from the CVSD encoder, or the T_X Data register, or the T_X 1010 Generator. Source selection is done through the μP port.
18	V_{CC}	Supply input for the audio sections, filters, and CVSD blocks. Allowable range is 2.7 to 5.5 V. Internally connected to Pins 27 and 37.
19	Enc In	The analog input to the CVSD encoder. Max. input level is 3.0 V_{pp}.
20	T_X Audio Out	Output of the transmit speech processing section.
21	Ground	Ground for the audio sections, filters, and CVSD blocks. Internally connected to Pins 30 and 40.
22	MCO	Output of the microphone amplifier, and input to the filters. This output has rail–to–rail capability.
23	MCI	Inverting input of the microphone amplifier. Gain and frequency response is set with external resistors and capacitors.
24	Enc Cap	This capacitor sets the time constant for the CVSD encoder. This pin is sensitive to leakage.
25	VAG	Analog ground for the audio section and the CVSD encoder and decoder.
26	Dec Cap	The capacitor sets the time constant for the CVSD decoder. This pin is sensitive to leakage.
27	V_{CC}	Supply input for the audio sections, filters, and CVSD blocks. Allowable range is 2.7 to 5.5 V. Internally connected to Pins 18 and 37.
28, 29	PAO+, PAO–	Differential outputs of the power amplifier stage for driving an earpiece or hybrid network. The gain and frequency response are set with external resistors and capacitors.
30	Gnd	Ground for the audio sections, filters, and CVSD blocks. Internally connected to Pins 21 and 40.
31	PAI	Input to the power amplifier stage. This pin is a summing node.
32	R_X Audio Output	Output of the receive speech processing section.
33	VB	The capacitor filters the internal 1.5 V reference voltage. If VB is adjusted, it may be monitored at this pin. Max. load current is 10 μA.
34	R_X Audio In	Input to the receive speech processing section.
35	Dec Out	The analog output of the CVSD decoder.
36	MP1	As an output, provides the recovered R_X data, or the Data Detect output, or the data slicer output. Or it can be set to a high impedance input (600 kΩ) for the carrier detect input signal. Selection is done through the μP port. See Table 6.
37	V_{CC}	Supply input for the audio sections, filters, and CVSD blocks. Allowable range is 2.7 to 5.5 V. Internally connected to Pins 18 and 27.
38	R_X Digital Input	The digital stream from the RF receiver is applied to the data slicer at this pin. Minimum amplitude is 200 mVpp. Hysteresis ≈50 mV.
39	MP2	As an output, this pin provides the recovered clock from the Clock Recovery block. As an input, the CVSD decoder clock can be applied to this pin. Or this pin may be set to a disabled state. Selection is done through the μP port. See Table 7. In Data Modem mode, the data to be transmitted is input to this pin.
40	Gnd	Ground for the audio sections, filters, and CVSD blocks. Internally connected to Pins 21 and 30.
41	LO2 Out	Buffered output of the 2nd LO frequency. A pullup resistor is required.
42	LO2 V_{CC}	Supply pin for the 2nd LO. Allowable range is 2.7 to 5.5 V.
43, 45	LO2+, LO2–	A tank circuit is connected to these pins for the 2nd LO.
44	LO2 Ctl	The varactor control pin for the 2nd LO.
46	LO2 Gnd	Ground for the 2nd LO section.
47	LO2 PD	Phase detector charge pump output of the 2nd LO PLL.
48	LO2 Gnd	Ground for the 2nd LO section.

NOTE: 1. All V_{CC} pins must be within ±0.5 V of each other.

Note: In the following descriptions, control bits in the MPU Serial Interface for the various functions will be identified by register number and bit number. For example, bit 3/19 indicates bit 19 of register 3. Bits 5/14–11 indicates register 5, bits 14 through 11. Please refer to Figure 1.

Transmit Speech Processing Section

This section is made up of the externally adjustable microphone amplifier (Pins 22 to 23), internally adjustable gain stage, two low pass filters, and a mute switch.

The gain of the microphone amplifier is set with external resistors to receive the audio from the microphone (in the handset), or from the hybrid (in the base unit), or from any other audio source. The MCO output has rail–to–rail capability, and the dc bias level is at VB (≈1.5 V).

The adjustable gain stage, referred to as the Remote Gain Adjust, provides 5 levels of gain in 4.0 dB increments. It is controlled with bits 6/15–11 as shown in Table 1.

Table 1. Remote Gain Adjust

Register 6 Bits 15–11	Gain
00001	–8.0 dB
00010	–4.0 dB
00100	0 dB
01000	+4.0 dB
10000	+8.0 dB

Other combinations for the 5 bits are invalid.

The Low Pass Filter after the gain stage is a switched capacitor filter with a corner frequency at 5.0 kHz. The subsequent smoothing low pass filter has a corner frequency at 30 kHz, and is designed to filter out high frequency clock noise from the previously mentioned switched capacitor filter.

The mute switch at Pin 20 will mute a minimum of 60 dB. Bit 6/2 controls the mute.

CVSD Encoder/Idle Channel/T_X Data Register

The analog signals to be digitized are input at Pin 19 to the CVSD Encoder. The output of the encoder will be the digital equivalent of the audio, at the selected clock rate. Based on the reference frequency, bits 4/23–18 are used to set the 6 Bit Encoder Counter, in conjunction with the subsequent ÷16 divider, to set the CVSD Encoder frequency to 32, 50, or 64 kHz. Bits 3/16–15 will set the CVSD for proper operation at the selected frequency, according to Table 2.

Table 2. CVSD Clock/Data Rates

Register 3		
Bit 16	Bit 15	Clock/Data Rate
0	1	32 kHz
1	0	50 kHz
1	1	64 kHz

The Encoder's minimum step size can be selected using bits 2/22–21, according to Table 3.

Table 3. Minimum Step Size

Encoder Register 2 Bits 22, 21	Decoder Register 1 Bits 22, 21	Step Size
00	00	No minimum
01	01	1.4 mV
10	10	5.6 mV
11	11	22.4 mV

The T_X 1010 Generator, when selected, provides an alternating "1–0" pattern (a square wave at half the CVSD clock rate) to the scrambler. This represents the lowest amplitude analog signal, and can be used when it is desired to send a quiet signal. Selection of this block can occur either automatically, or intentionally, as follows:

a. The automatic selection occurs when the Idle Channel Detector senses the average audio signal at Pin 19 is below a threshold which is set with bits 5/17–15 (See Table 4). Bits 5/14–11 select a time delay for the automatic threshold detection to occur. The minimum delay is zero, with these bits set to 0000. Changing the bits provides delay in increments of 32 clock cycles (of the CVSD Encoder clock). The maximum delay is 480 clock cycles, (7.5 mS at 64 kHz). When the average audio signal at Pin 19 increases above the threshold, the T_X 1010 Generator will be deselected with no delay. This automatic switchover feature can be disabled with bit 7/2. Bit 5/21 indicates when an idle channel condition has been detected. This output bit will be functional even when the idle channel detector is disabled with bit 7/2. Bit 5/18 will power down the Idle Channel Detect Circuit as a power saving measure.
b. Bit 6/4 can be used to intentionally select the T_X 1010 Generator at any time.

Table 4. Idle Channel Detection Threshold

Register 5 Bits 17–15	Threshold		Register 5 Bits 17–15	Threshold
000	–50 dBV		100	–60 dBV
001	–52.5		101	–62.5
010	–55		110	–65
011	–57.5		111	–67.5

The T_X Data Register is used for the transmission of data between the handset and base units. The procedure is as follows:

a. At the receiving unit: The code word (16 or 24 bits, set with bit 7/11) identifying that a data transmission is occurring must be loaded into the T_X Data Register (by loading register 8). This is used to detect when a code word is sent from the transmitting unit.
b. At the transmitting unit: The same code word as above is loaded into register 8. It is automatically loaded into the T_X Data Register.
c. The data word (16 or 24 bits, set with bit 7/12) is then loaded into register 9.

d. Upon loading register 9, the MC33410 automatically sends out (at Pin 17) the code word, followed by the data word, at the CVSD clock rate.

When the data word is completely sent out, the MC33410 will then return Pin 17 to its previous source of digital information (CVSD Encoder or T_X 1010 Generator).

Scrambler/Digital Output

The scrambler receives digital data from the CVSD Encoder, or the T_X 1010 Generator, or the T_X Data Register, to be output at Pin 17. The output level is 0 to V_{CC}. The scrambler can be bypassed with Bit 7/1.

The scrambler, better known as a randomizer, provides not only a level of communication security, but also helps ensure the digital output will not contain an abnormally long string of 1s or 0s which can adversely affect the CVSD Decoder operation, as well as the RF section. The scrambler is a maximal–length shift register sequence generator. The length of the shift register is selectable to one of eight values with bits 7/10–8 (the descrambler in the receiving unit must be set the same). Table 5 lists the polynomial associated with each tap selection.

Table 5. Scrambler/Descrambler Tap Selection

Tap No.	Register 7			Shift Register Length	Polynomial
	Bit 10	Bit 9	Bit 8		
0	0	0	0	2	$1 + z^{-1} + z^{-2}$
1	0	0	1	3	$1 + z^{-2} + z^{-3}$
2	0	1	0	4	$1 + z^{-3} + z^{-4}$
3	0	1	1	5	$1 + z^{-3} + z^{-5}$
4	1	0	0	6	$1 + z^{-5} + z^{-6}$
5	1	0	1	7	$1 + z^{-6} + z^{-7}$
6	1	1	0	9	$1 + z^{-5} + z^{-9}$
7	1	1	1	10	$1 + z^{-7} + z^{-10}$

Data Slicer/Clock Recovery

The data slicer will receive the low level digital signal from the RF receiver section at Pin 38. The input signal to the data slicer must be >200 mVpp. Hysteresis of 50 mV is internally provided. The output of the data slicer will be same waveform, but with an amplitude of 0 to V_{CC}, and can be observed at Pin 36 (MP1) if bits 7/5–4 are set to 10. The output can be inverted by setting bit 5/19 = 1.

The clock recovery block will generate a phase locked clock, equal to the CVSD data rate, from the incoming data, as long as the Encoder Counter (bits 4/23–18) is set for that data rate. The recovered clock can be observed at Pin 39 (MP2) if bits 7/7–6 are set to 00. The data from the clock recovery block can be observed at Pin 36 if bits 7/5–4 are set to 00. The clock recovery block may be bypassed by setting bit 7/0 to 1. With this setting the data slicer output will go directly to the descrambler, and the encoder clock will replace the Clock Recovery Clock.

Tables 6 and 7 summarize the options available at MP1 and MP2 (Pins 36 and 39).

Table 6. MP1 Options (Pin 36)

Register 7		Function
Bit 5	Bit 4	
0	0	Data from clock recovery block
0	1	Data Detect Output
1	0	Data Slicer Output
1	1	Hi–Z/ CD Input

Table 7. MP2 Options (Pin 39)

Register 7		Function
Bit 7	Bit 6	
0	0	Output recovered clock
0	1	Input CVSD Decoder clock
1	X	Disabled (Hi–Z)

When MP1 is set to a Hi–Z condition, the pin is an input for the CD (Carrier Detect) function, with an input impedance of 600 KΩ. See the section entitled Low Battery/Carrier Detect for an explanation of this function.

Descrambler

The descrambler receives the scrambled data from the clock recovery block (or the data slicer if bit 7/0 = 1), and descrambles it to the original data as long as the selected taps are the same as those in the transmitting scrambler (see Table 5). The descrambler block is the same configuration as the scrambler, and is self–synchronizing. The descrambler can be bypassed with bit 7/1.

Data Detect Register/Status Output/R_X Data Register

The Data Detect register will continuously compare the descrambled data it receives with the 16 or 24–bit code word stored in the T_X Data Register (loaded through register 8). Upon detecting a match, and after the code word passes through the shift register, the following (16 or 24–bit) data word will be stored into the R_X Data Register, and then loaded into register 10 of the MPU Interface. At this time the Status

output at Pin 13, and bit 5/22, will go high. The external microprocessor can then retrieve the data word by reading register 10, at which time the Status pin and bit will go low.

Upon detection of a code word as described above, the CVSD Decoder will be provided with 32, 40, or 48–bits of a 1010 pattern (idle channel) to minimize disturbances to the audio. After the data word is loaded into register 10, the CVSD Decoder resumes receiving data from the descrambler. The audio is therefore interrupted with a low level signal for a maximum of 48 clock cycles (0.75 mSec at 64 kHz).

The Data Detect register can be bypassed by setting bit 7/3 = 1.

CVSD Decoder/Decoder Clock/Idle Channel

The CVSD Decoder will provide the analog equivalent, at Pin 35, of the digital data it receives from the descrambler, or from the 1010 generator (idle channel generator). There is a single pole filter at the Decoder output to reduce the clock noise normally present on a CVSD analog output. The CVSD Decoder is self synchronizing as long as the decoder clock matches the data rate, and the Decoder has been set with bits 3/16–15 according to Table 2.

The Decoder clock is provided from the Clock Recovery block by setting bits 7/7–6 to 00 or 1X. The clock is internally provided to the Decoder, and is available at Pin 39. Alternately, a Decoder clock can be provided from an external source to Pin 39 by setting bit 7/7–6 to 01 (see Table 7).

The R_X 1010 Generator provides an alternating 1–0 pattern (a square wave at half the CVSD clock rate) to the CVSD Decoder, resulting in the lowest amplitude analog signal at Pin 35. The 1010 Generator is automatically selected whenever data is detected and received by the Data Detection Circuit, as described above. Additionally, the 1010 Generator can be selected with bit 6/3 at any time.

The Decoder's minimum step size can be selected using bits 1/22–21, according to Table 3.

Receive Audio Path

The Receive Audio Path (Pins 34 to 32) consists of an anti–aliasing filter, a low pass filter, a gain adjust stage, and a mute switch.

Since the analog output of the CVSD Decoder (typically input at Pin 34) will contain noise at the CVSD clock rate, the anti–aliasing filter, with a corner frequency at 30 kHz, is provided to prevent aliasing of that clock noise with the subsequent switched capacitor filter.

The switched capacitor low pass filter is a 3 pole filter, with a corner frequency at 5.0 kHz. This is designed to remove the clock noise from the CVSD Decoder output signal, as well as provide bandwidth limiting in the audio range.

The gain stage provides 28.5 dB of gain adjustment in 19 steps (1.5 dB each), measured from Pin 34 to 32. Bits 6/10–6 are used to set the gain according to Table 8.

The mute switch at Pin 32, controlled by bit 6/1, will mute a minimum of 60 dB.

Table 8. Receive Gain Adjustment

Register 6 Bits 10...6	Gain		Register 6 Bits 10...6	Gain
00110	–13.5 dB		10000	+1.5 dB
00111	–12.0 dB		10001	+3.0 dB
01000	–10.5 dB		10010	+4.5 dB
01001	–9.0 dB		10011	+6.0 dB
01010	–7.5 dB		10100	+7.5 dB
01011	–6.0 dB		10101	+9.0 dB
01100	–4.5 dB		10110	+10.5 dB
01101	–3.0 dB		10111	+12.0 dB
01110	–1.5 dB		11000	+13.5 dB
01111	0.0 dB		11001	+15.0 dB

Power Amplifiers

The power amplifiers (Pins 28, 29, 31) are designed to drive the earpiece in a handset, or the telephone line via a hybrid circuit in the base unit. Each output (PAO+ and PAO–) can source and sink 5 mA, and can swing 2.0 V_{pp} each. The gain of the amplifiers is set with a feedback resistor from Pin 29 to 31, and an input resistor at Pin 31. The differential gain is 2x the resistor ratio. Capacitors can be used for frequency shaping. The pins' dc level is VB (≈1.5 V).

The Mute switch, controlled with bit 6/0, will provide 90 dB of muting with a 50 kΩ feedback resistor. The amount of muting will depend on the value of the feedback resistor.

Reference Clock

The reference clock provides the frequency basis for the three PLLs, the switched capacitor filters, and the CVSD Encoder section. The source for the reference clock can be a crystal in the range of 4.0 to 18.25 MHz connected to Pins 14 & 15, or it can be an external source connected to F_{ref} In (Pin 14). The reference frequency is directed to:

a. A programmable 12–bit counter to provide the reference frequency for the three PLLs. The 12–bit counter is to be set such that, in conjunction with the programmable counters within each PLL, the proper frequencies can be produced by each VCO.
b. A programmable 6–bit counter, followed by a ÷2 stage, to set the frequency for the switched capacitor filters to 256 kHz, or as close to that as possible.
c. A programmable 6–bit counter which provides the 16x clock for the Clock Recovery block. This is followed by a ÷16 stage which provides the CVSD Encoder clock. This is followed by a ÷32 stage, and a programmable 4–bit counter which sets the delay for the Idle Channel Detect circuit.

Transmit and Receive (LO1) PLL Sections

The transmit and receive PLLs (Pins 6 to 9 and 1 to 4, respectively) are designed to be part of a 900 MHz system. In

a typical application the Transmit PLL section will be set up to generate the transmit frequency, and the Receive PLL section will be set up to generate the LO1 frequency. The two sections are identical, and function independently. External requirements for each include a low pass filter, a 900 MHz VCO, and a 64/65 or 128/129 dual modulus prescaler.

The frequency output of the VCO is to be reduced by the dual modulus prescaler, and then input to the MC33410 (at Pin 2 or 8). That frequency is then further reduced by the programmable 13–bit counter (bits 1/19–7 or 2/19–7), and provided to one side of the Phase Detector, where it is compared with the PLL reference frequency. The output of the phase detector (at Pin 4 or 6) is a bi–directional charge pump which drives the VCO through the low pass filter. Bits 1/20 and 2/20 set the gain of each of the two charge pumps to either 100/2π μA/Radian or 400/2π μA/Radian. The polarity of the two phase detector outputs is set with bits 7/22 and 7/23. If the bit=0, the appropriate PLL is configured to operate with a non–inverting low pass filter/VCO combination. If the low pass filter/VCO combination is inverting, the polarity bit should be set to 1.

The 7–bit A and A' counters (bits 1/6–0 and 2/6–0) are to be set to drive the Modulus Control input of the 64/65 or 128/129 dual modulus prescalers. The Modulus Control outputs (Pins 1 and 9) can be set to either a voltage mode or a current mode with bit 7/13.

To calculate the settings of the N and A registers, the following procedure is used:

$$\frac{f_{VCO}}{f_{PLL}} = Nt \text{ (Nt must be an integer)} \qquad \text{Equation 1}$$

$$\frac{Nt}{P} = N \qquad \text{Equation 2}$$

A = Remainder of Equation 2 (decimal part of N x P) Equation 3

where: f_{VCO} = the VCO frequency
f_{PLL} = the PLL Reference Frequency set within the MC33410
P = the smaller divisor of the dual modulus prescaler (64 for a 64/65 prescaler)
N = the whole number portion is the setting for the N (or N') counter within the MC33410
A = the setting for the A (or A') counter within the MC33410

For example, if the VCO is to provide 910 MHz, and the internal PLL reference frequency is 50 kHz, then the equations yield:

$$Nt = \frac{910 \times 10^6}{50 \times 10^3} = 18,200$$

$$N = \frac{18,200}{64} = 284.375$$

$$A = 0.375 \times 64 = 24$$

The N register setting is 284_d (0 0001 0001 1100), and the A register setting is 24_d (001 1000).

2nd LO (LO2)

This PLL is designed to be the 2nd Local Oscillator in a typical 900 MHz system, and is designed for frequencies up to 80 MHz. The VCO and varactor diodes are included, and are to be used with an external tank circuit (Pins 43 to 45).

Bits 7/20–18 are used to select an internal capacitor, with a value in the range of 0 to 7.6 pF, to parallel the varactor diodes and the tank's external capacitor. This permits a certain amount of fine tuning of the oscillator's performance. See Table 9.

A buffered output is provided to drive, e.g., a mixer. The frequency is set with the programmable 14–bit counter (bits 3/13–0) in conjunction with the PLL reference frequency. For example, if the reference frequency is 50 kHz, and the 2nd LO frequency is to be 63.3 MHz, the 14–bit counter needs to be set to 1266_d (00 0100 1111 0010). The output level is dependent on the value of the impedance at Pin 41, partly determined by the external pullup resistor.

The output of the phase detector is a bi–directional charge pump which drives the varactor diodes through an external low pass filter. Bit 3/14 sets the gain of the charge pump to either 100/2π μA/Radian or 400/2π μA/Radian. Bit 7/21 sets its polarity – if 0, the PLL is configured to operate with a non–inverting low pass filter/VCO combination. If the low pass filter/VCO combination is inverting, the polarity bit should be set to 1.

Table 9. LO2 Capacitor Selection

Register 7 Bits 20–18	Capacitor Value		Register 7 Bits 20–18	Capacitor Value
000	0 pF		100	4.3 pF
001	1.1 pF		101	5.4 pF
010	2.2 pF		110	6.5 pF
011	3.3 pF		111	7.6 pF

VB Reference Voltage

The VB voltage (≈1.5 V) is available at Pin 33. It will have a production tolerance of ±6%, and can be adjusted over a ±9% range using bits 3/20–17. The adjustment steps will be ≈1.2% each. VB can be used to bias external circuitry, as long as the load current on this pin does not exceed 10 μA.

Low Battery/Carrier Detect

This circuit will provide an indication of either Low Battery voltage, or a low carrier signal applied to Pin 36 (MP1) from an RSSI circuit. The desired mode is selected with bit 6/5.

A) Low Battery Mode (Bit 6/5 = 0)

The supply voltage at Pin 18 is applied to the comparator through an internal resistor divider, and is compared to the internal reference VB (≈1.5 V). The comparator has ≈15 mV of hysteresis, measured at V_{CC}. The resistor divider is adjustable using bits 3/23–21. The Low Battery threshold voltage will then be equal to the VB voltage multiplied by the factor listed in Table 10. For example, if VB = 1.5 V, and bits 3/23–21 = 011, the threshold will be 3.21 V.

B) Carrier Detect Mode (Bit 6/5 = 1)

Pin 36 (MP1) must be set to the Hi–Z/CD Input mode by setting bits 7/5–4 to 11. MP1 will then be an input with an input impedance of ≈600 kΩ, referenced to VB. An analog signal applied to MP1 will be applied to the comparator through an internal adjustable gain stage (adjustable using bits 3/23–21), and is compared to the internal reference VB. The comparator has ≈18.0 mV of hysteresis, measured at Pin 36. The threshold voltage will then be equal to the VB voltage multiplied by the factor listed in Table 10. For

example, if VB = 1.5 V, and bits 3/23–21 = 011, the threshold will be 0.576 V.

Table 10. LB/CD Threshold Adjustment Factor

Register 3 Bits 23–21	Low Battery Mode	Carrier Detect Mode
000	1.96	0.574
001	2.02	0.524
010	2.08	0.453
011	2.14	0.384
100	2.19	0.314
101	2.25	0.247
110	2.30	0.177
111	2.37	0.110

The comparator output is at bit 5/23, and at Pin 16 (open collector output). The outputs are high if the monitored V_{CC} voltage is above the threshold, or if the Carrier signal is below the threshold. Pin 16 requires an external pullup resistor. When this circuit is disabled (bit 5/10 = 1), bit 5/23 and Pin 16 will be high.

MPU Serial Interface

The MPU Serial Interface is a 3–wire interface, consisting of a Clock line, an Enable line, and a bi–directional Data line. The interface is always active, i.e. it cannot be powered down as all other sections of the MC33410 are disabled and enabled through this interface.

The clock must be supplied to the MC33410 at Pin 11 to write or read data, and can be any frequency up to 2.0 MHz. The clock need not be present when data is not being transferred. The Enable line must be low when data is not being transferred.

Internally there are 10 data registers, 24 bits each, addressed with four bits ranging from $1 to $A. Register 10, and bits 23–21 of register 5 contain data to be read out by the microprocessor, while all other register bits are to be written to by the microprocessor. The contents of the 10 registers can be read out at any time. All bits are written in, or read out, on the clock's positive transition. The write and read operations are as follows:

a) Write Operation:

To write data to the MC33410, the following sequence is required (see Figure 2):

1. The Enable line is taken high.
2. Five bits are entered:
   - The first bit must be a 0 to indicate a Write operation.
   - The next four bits identify the register address (0001–1010). The MSB is entered first.
3. After the 5th clock pulse is low, the Enable line is taken low. At this transition, the address is latched in and decoded.
4. The Enable line is maintained low while the data bits are clocked in. The MSB is entered first, and the LSB last. If 24 bits are written to a register which has less than 24 active bits (e.g., register 6), the unassigned bits are to be 0.
5. After the last bit is entered, the Enable line is to be taken high and then low. The falling edge of this pulse latches in the just entered data. The clock line can be at a logic high or low, but must not transition in either direction during this Enable pulse.
6. The Enable line must then be kept low until the next communication.

Note: If less than 24 bits are to be written to a data register, it is not necessary to enter the full 24 bits, as long as they are all lower order bits. For example, if bits 0–6 of a register are to be updated, they can be entered as 7 bits with 7 clock cycles in step 4 above. However, if this procedure is used, a minimum of 4 bits, with 4 clock pulses, must be entered.

Figure 2. Writing Data to the MC33410

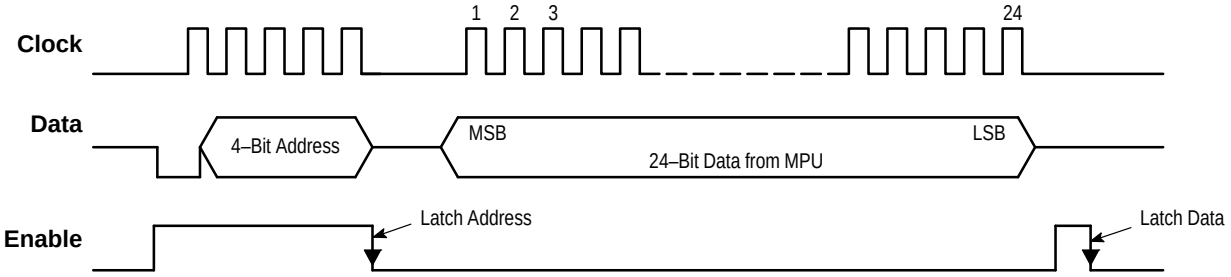
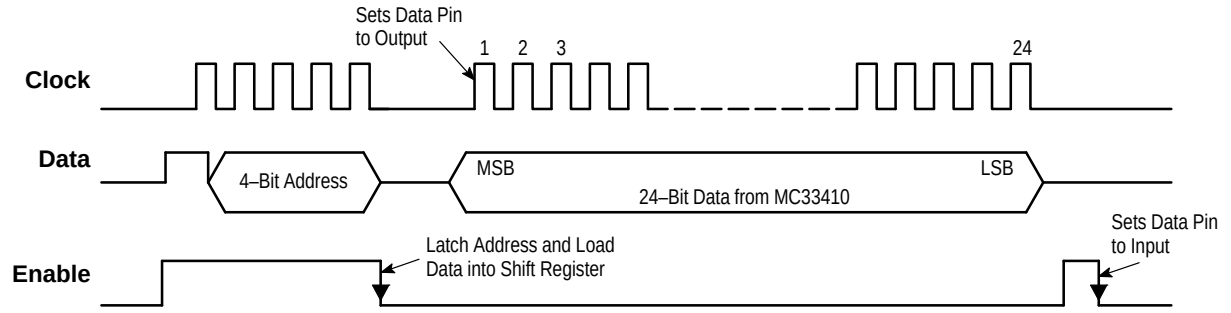


Figure 3. Reading Data from the MC33410



b) Read Operation:

To read the output bits (bits 5/23–21, or all of register 10), or the contents of any register, the following sequence is required (see Figure 3):

1. The Enable line is taken high.
2. Five bits are entered:
   – The first bit must be a 1 to indicate a Read operation.
   – The next four bits identify the register address (0001–1010). The MSB is entered first.
3. After the 5th clock is taken low, the Enable line is taken low. At this transition, the address is latched in and decoded, and the contents of the selected register is loaded into the 24–bit output shift register. At this point, the Data line (Pin 12) is still an input.
4. While maintaining the Enable line low, the data is read out. The first clock rising edge will change the Data line to an output, and the MSB will be present on this line.
5. The full contents of the register are then read out (MSB first, LSB last) with a total of 24 clock rising edges, including the one in step 4 above. It is recommended that the MPU read the bits at the clock's falling edge. If only bit 23, 22, or 21 of register 5 are to be read, this can be done with one, two, or three clock rising edges, respectively.
6. After the last clock pulse, the Enable line is to be taken high and then low. The falling edge of this pulse returns the Data pin to be an input. The clock line can be at a logic high or low, but must not transition in either direction during this Enable pulse.
7. The Enable line must then be kept low until the next communication.

Data Modem Mode

For applications where the MC33410 is to be used in a 900 MHz wireless system for transmitting data only (non–voice), a mode can be set which bypasses the speech digitizing sections. The resulting configuration makes use of those sections associated with data only, i.e., the scrambler, descrambler, and clock recovery section. Also functional are the three PLLs, the audio receive path (Pins 34 to 28), the transmit audio path (Pins 23 to 20), and the Low Battery circuit (but not the Carrier Detect mode).

In this mode, the MC33410 will provide the transmit data clock from the crystal, in conjunction with the internal 6–bit counter (bits 4/23–18) and the ÷16 block associated with that counter. The transmit data clock is available at Pin 13, and can be used to synchronize the external data source. The T_X data is input at Pin 39, passes through the scrambler, and outputs at Pin 17.

The demodulated data from the RF receiver is input at Pin 38, and is applied to the data slicer, and the clock recovery block. The recovered clock is output at Pin 12. The data passes through the descrambler, and is output at Pin 36.

Figure 4 is a diagram of the data paths through the MC33410.

The procedure for entering the Data Modem mode is in Table 11:

Table 11. Entering Data Modem Mode

Function	Bits	Bit Value
Set T_X Clock to desired frequency T_X Clk = $F_{crystal}$/(16 x Counter).	4/23 – 18	As Desired
Set Scrambler & Descrambler tap setting (Bit 7/1 = 0).	7/10 – 8	As Desired
Bypass Data Detect.	7/3	1
Set MP1 to Data Detect Output.	7/5 – 4	01
Set Test Mode bits to connect Encode Clock to Status (Pin 13).	7/17 – 15	110
Set Data Modem Mode (MP2 to scrambler Input).	5/20	1
Write to Register 11 as shown in Figure 5 to configure Pin 12.	N/A	N/A

The above sequence is not critical, except that the last two steps must be the setting of bit 5/20, and writing to register 11. Writing to register 11 is shown in Figure 5.

Figure 4. Data Modem Mode Configuration

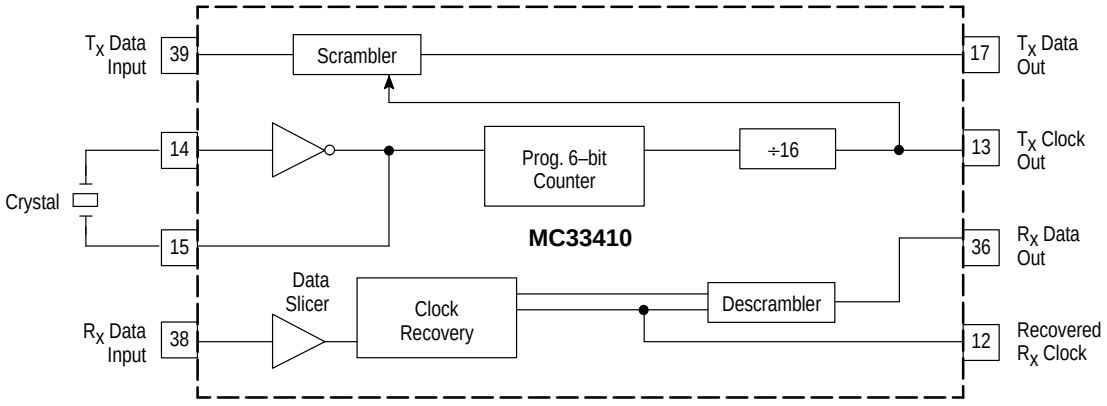
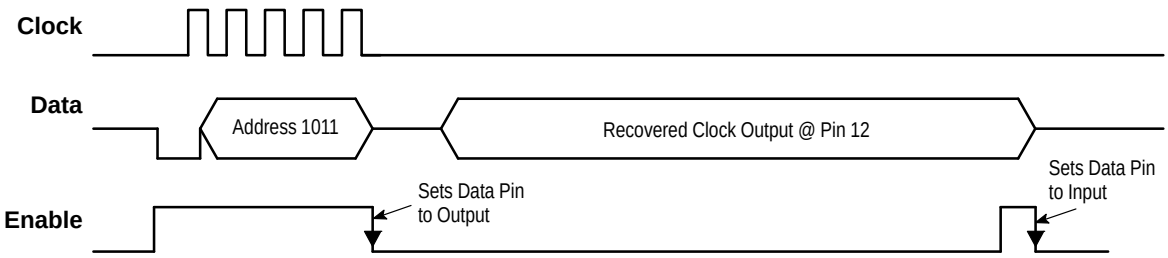


Figure 5. Entering/Exiting Data Modem Mode



After address 11 is clocked in, the Enable falling edge will cause Pin 12 (Data) to switch to an output, providing the recovered clock. The microprocessor's data pin must be changed to an input prior to this falling edge. This sequence is effective only if bit 5/20 is set to a 1.

During the time that recovered clock is available at Pin 12, the microprocessor port is unavailable for any control functions.

To exit the Data Modem mode, the Enable line is to be taken high and low (the clock is to be stable during this active high pulse). The falling edge will set Pin 12 to be an input, allowing normal use of the microprocessor port. The next step is to set bit 5/20 to a 0. Other register bits can then be set as needed.

To prevent inadvertent incorrect operation of the microprocessor port, bit 5/20 must always be set to 0 when the Data Modem mode is not in use.

Power Supply/Power Saving Modes

The power supply voltage, applied to all V_{CC} pins, can range from 2.7 to 5.5 V. All V_{CC} pins must be within ±0.5 V of each other, and each must be bypassed. It is recommended a ground plane be used, and all leads to the MC33410 be as short and direct as possible. The supply and ground pins are distributed as follows:

1. Pins 18, 27 and 37 are internally connected together, and provide power to the audio amplifiers, filters, CVSD encoder and decoder, and the low frequency (CVSD rate) logic circuits. Pins 21, 30 and 40 are the ground pins for these sections.
2. Pin 3 provides power to the R_X PLL section. Pin 5 is the ground pin.
3. Pin 7 provides power to the T_X PLL section, and the MPU interface. Pin 5 is the ground pin.
4. Pin 42 provides power to the 2nd LO section. Pins 46 and 48 are the ground pins.

To conserve power, various sections can be individually disabled, using bits 5/10–0 (setting a bit to 1 disables the section).

1. Reference Oscillator Disable (bit 5/0) – The reference oscillator at Pins 14 and 15 is disabled, thereby denying a clock to the three PLLs, the CVSD Encoder, and the switched capacitor filters.
2. T_X PLL Disable (bit 5/1) – The 13–bit and 7–bit counters, input buffer, phase detector, and modulus control blocks are disabled. The charge pump output at Pin 6 will be in a Hi–Z state.
3. R_X PLL Disable (bit 5/2) – The 13–bit and 7–bit counters, input buffer, phase detector, and modulus control blocks are disabled. The charge pump output at Pin 4 will be in a Hi–Z state.
4. LO2 PLL Disable (bit 5/3) – The VCO, 14–bit counter, output buffer, and phase detector are disabled. The charge pump output at Pin 47 will be in a Hi–Z state.
5. R_X Data Path Disable (bit 5/4) – The data slicer, clock recovery block, descrambler, data detect register, and the status output circuit are disabled. The state of the status line (Pin 13 and bit 5/22) will not change upon disabling this section.
6. CVSD Decoder Disable (bit 5/5) – The CVSD Decoder and the R_X 1010 Generator are disabled.
7. R_X Audio Path Disable (bit 5/6) – The anti–aliasing filter, low pass filter, and variable gain stage are disabled.
8. Power Amplifier Disable (bit 5/7) – The two power amplifiers are disabled. Their outputs will go to a Hi–Z state.
9. T_X Audio Path Disable (bit 5/8) – Disables the microphone amplifier, low pass filter, and smoothing filter.
10. CVSD Encoder Disable (bit 5/9) – The CVSD Encoder, Idle Channel detect circuit, the T_X 1010 Generator, the T_X Data register, and the scrambler are disabled.
11. Low Battery/Carrier Detect Disable (bit 5/10) – The LB/CD circuit is disabled. The output, at bit 5/23 and Pin 16 will be at a logic high.
12. Idle Channel Detect Disable (bit 5/18) – Powers down the Idle Channel Detect circuit.

Note: The 12–bit reference counter is disabled if the three PLLs are disabled (bits 5/1–3 = 1).

Table 12. Control Bit Listing (By Register Number)

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
1 (23 bits total)	6 – 0	1000000	Sets the 7–bit T_X A counter for the T_X PLL.
	19 – 7	10....0	Sets the 13–bit T_X N counter for the T_X PLL.
	20	0	Sets the T_X phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
	22, 21	00	Sets CVSD Decoder minimum step size per Table 3.
2 (23 bits total)	6 – 0	1000000	Sets the 7–bit R_X A' counter for the R_X PLL.
	19 – 7	10....0	Sets the 13–bit R_X N' counter for the R_X PLL.
	20	0	Sets the R_X phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
	22, 21	00	Sets CVSD Encoder minimum step size per Table 3.
3 (24 bits total)	13 – 0	10....0	Sets the 14–bit counter for the 2nd LO.
	14	0	Sets the LO2 phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
	16 – 15	11	Set the CVSD encoder/decoder for the selected clock rate. (Table 2)
	20 – 17	0111	Adjusts the VB reference voltage (≈1.5 V) to improve low battery detection accuracy. Total adjustment range is ≈±9%.
	23 – 21	011	Selects the threshold for Low Battery Detection or Carrier Signal Detection. See Table 10.
4 (24 bits total)	11 – 0	$800	Sets the 12–bit counter for the PLL Reference Clock.
	17 – 12	100000	Sets the 6–bit counter for the Switched Capacitor Filter clock.
	23 – 18	100000	Sets the 6–bit counter to set the CVSD Encoder clock rate.
5 (24 bits total)	0	0	Power down the Reference Oscillator
	1	0	Power down the T_X PLL.
	2	0	Power down the R_X PLL.
	3	0	Power down the LO2 PLL.
	4	0	Power down the R_X Data Path. Includes Data Slicer, Clock Recovery, Descrambler, Data Detect, and Status circuits.
	5	0	Power down the CVSD Decoder.
	6	0	Power down the R_X Audio path (Pin 32 to 30). Includes AALPF, LPF, and Gain Adjust circuits.
	7	0	Power down the Power Amplifiers (Pins 27, 28)
	8	0	Power down the T_X Audio Path (Pin 25 to 22). Includes micro–phone amplifier, LPF, and Smoothing LPF circuits.
	9	0	Power down the CVSD Encoder, Idle Channel Detector, 1010 Generator, T_X Data Register, and Scrambler circuits.
	10	0	Power down the Low Battery/Carrier Detect Circuit.
	14 – 11	0111	Sets the 4–bit counter to set the response delay for the idle channel detect circuit.
	17 – 15	100	Sets the idle channel detect threshold level. See Table 4.
	18	0	Power down the Idle Channel Detect Circuit.
	19	0	Inverts the Data Slicer output.
	20	0	Sets the Data Modem mode of operation.
	21	N/A	Indicates an idle channel condition has been detected (Output). This output is unaffected by bit 7/2.
	22	N/A	The Status Output (same as Pin 13) is read out from this bit.
	23	N/A	The output of the Low Battery/Carrier Detect Circuit is read from this bit.

Table 12. Control Bit Listing (By Register Number) (continued)

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
6 (16 bits total)	0	0	Mutes the power amplifiers (Pins 27 to 29).
	1	0	Mutes the receive speech processing path (Pin 30).
	2	0	Mutes the transmit speech processing path (Pin 22).
	3	0	Selects the R_X 1010 Generator to the CVSD decoder.
	4	0	Selects the T_X 1010 Generator to the scrambler.
	5	0	Sets Carrier Detect Mode vs. Low Battery mode.
	10 – 6	01111	Provides 19 steps, 1.5 dB each (28.5 dB range), of gain adjust in the receive speech audio path (Pins 32 to 30). See Table 8.
	15 – 11	00100	Provides 4 steps of 4.0 dB each, for the remote gain adjust in the transmit speech audio path (Pins 23 to 20).
7 (24 bits total)	0	0	Bypass the Clock Recovery Block (Data slicer output goes directly to the descrambler).
	1	0	Bypass the scrambler and descrambler.
	2	0	Disables the automatic idle channel detect at the CVSD encoder. Bit 5/21 is still active.
	3	0	Bypass the Data Detect block (Descrambler output goes directly to the CVSD Decoder).
	5 – 4	00	Determines the function for Pin 36 (MP1). See Table 6.
	7 – 6	00	Determines the function for Pin 39 (MP2). See Table 7.
	10 – 8	010	Selects one of 8 programmable taps in the scrambler and descrambler. See Table 5.
	11	1	Sets the code word size to be sent out via the T_X Data Register to 24 bits. If this bit is 0, the code word size is 16 bits.
	12	1	Sets the data word size to be sent out via the T_X Data Register to 24 bits. If this bit is 0, the data word size is 16 bits.
	13	0	Sets the FT_X MC and FR_X MC output level to be from ground to V_{CC}. If this bit is 0, the output level is ±100 μA.
	14	0	Disables the CVSD charge compensation circuit.
	17 – 15	000	Test modes for production testing only.
	20 – 18	000	Selects the value of the internal capacitor between Pins 43 to 45, to fine tune the LO2 tank circuit. See Table 9.
	21	0	Sets the polarity of the 2nd LO phase detector charge pump output for an inverting low pass filter/VCO combination.
	22	0	Sets the polarity of the R_X phase detector charge pump output for an inverting low pass filter/VCO combination.
	23	0	Sets the polarity of the T_X phase detector charge pump output for an inverting low pass filter/VCO combination.
8	23 – 0	$000000	Code word for the T_X Data Register is entered into this register.
9	23 – 0	$000000	Data word for the T_X Data Register is entered into this register.
10	23 – 0	$000000	The data word received into the R_X Data Register is read out via the μP port from this register.

Table 13. Control Bit Listing (By Function)

PLL Controls

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
1	6 – 0	1000000	Sets the 7–bit T_X A counter for the T_X PLL.
1	19 – 7	10....0	Sets the 13–bit T_X N counter for the T_X PLL.
2	6 – 0	1000000	Sets the 7–bit R_X A' counter for the R_X PLL.
2	19 – 7	10....0	Sets the 13–bit R_X N' counter for the R_X PLL.
3	13 – 0	10....0	Sets the 14–bit counter for the 2nd LO.
4	11 – 0	$800	Sets the 12–bit counter for the PLL Reference Clock.
7	13	0	Sets the FT_X MC and FR_X MC output level to be from ground to V_{CC}. If this bit is 0, the output level is ±100 μA.

PLL Phase Detectors

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
1	20	0	Sets the T_X phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
2	20	0	Sets the R_X phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
3	14	0	Sets the LO2 phase detector charge pump output current. 0 = ±100 μA, and 1 = ±400 μA.
7	20 – 18	000	Selects the value of the internal capacitor between Pins 43 to 45, to fine tune the LO2 tank circuit. See Table 9.
7	21	0	Sets the polarity of the 2nd LO phase detector charge pump output for an inverting low pass filter/VCO combination.
7	22	0	Sets the polarity of the R_X phase detector charge pump output for an inverting low pass filter/VCO combination.
7	23	0	Sets the polarity of the T_X phase detector charge pump output for an inverting low pass filter/VCO combination.

CVSD Controls

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
1	22, 21	00	Sets CVSD Decoder minimum step size per Table 3.
2	22, 21	00	Sets CVSD Encoder minimum step size per Table 3.
3	16 – 15	11	Set the CVSD encoder/decoder for the selected clock rate. (Table 2)
4	23 – 18	100000	Sets the 6–bit counter to set the CVSD Encoder clock rate.
6	3	0	Selects the R_X 1010 Generator to the CVSD decoder.
6	4	0	Selects the T_X 1010 Generator to the scrambler.
7	14	0	Disables the CVSD charge compensation circuit, which affects idle channel performance.

Idle Channel Detector

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
5	14 – 11	0111	Sets the 4–bit idle channel counter to set the response delay for the idle channel detect circuit.
5	17 – 15	100	Sets the idle channel detect threshold level. See Table 4.
5	21	N/A	Indicates an idle channel condition has been detected (Output). This output is unaffected by bit 7/2.
7	2	0	Disables the automatic idle channel detect at the CVSD encoder. Bit 5/21 is still active.

Table 13. Control Bit Listing (By Function) (continued)

Data Transmission/Reception

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
5	19	0	Inverts Data Slicer output.
5	20	0	Sets Data Modem mode.
5	22	N/A	The Status Output (same as Pin 13) is read out from this bit. A logic 1 indicates the Data Detect register has detected a code word.
7	0	0	Bypass the Clock Recovery Block (Data slicer output goes directly to the descrambler).
7	3	0	Bypass the Data Detect block (Descrambler output goes directly to the CVSD Decoder).
7	11	1	Sets the code word size to be sent out via the T_X Data Register to 24 bits. If this bit is 0, the code word size is 16 bits.
7	12	1	Sets the data word size to be sent out via the T_X Data Register to 24 bits. If this bit is 0, the data word size is 16 bits.
8	23 – 0	$000000	Code word for the T_X Data Register is entered into this register.
9	23 – 0	$000000	Data word for the T_X Data Register is entered into this register.
10	23 – 0	$000000	The data word received into the R_X Data Register is read out via the µP port from this register.

Scrambler/Descrambler

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
7	1	0	Bypass the scrambler and descrambler.
7	10 – 8	010	Selects one of 8 programmable taps in the scrambler and descrambler. See Table 5.

Multi Purpose Pin Control

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
7	5 – 4	00	Determines the function for Pin 36 (MP1). See Table 6.
7	7 – 6	00	Determines the function for Pin 39 (MP2). See Table 7.

Audio Paths

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
4	17 – 12	100000	Sets the 6–bit counter for the Switched Capacitor Filter clock.
6	0	0	Mutes the power amplifiers (Pins 27 to 29).
6	1	0	Mutes the receive speech processing path (Pin 30).
6	2	0	Mutes the transmit speech processing path (Pin 22).
6	10 – 6	01111	Provides 19 steps, 1.5 dB each (28.5 dB range), of gain adjust in the receive speech audio path (Pins 32 to 30). See Table 8.
6	15 – 11	00100	Provides 4 steps of 4.0 dB each, of gain adjust in the transmit speech audio path (Pins 23 to 20).

Low Battery/Carrier Detection

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
3	20 – 17	0111	Adjusts the VB reference voltage (≈1.5 V) to improve low battery detection accuracy. Total adjustment range is ≈±9%.
3	23 – 21	011	Selects the threshold for Low Battery Detection or Carrier Signal Detection. See Table 10.
5	23	N/A	The output of the Low Battery/Carrier Detect Circuit is read from this bit.
6	5	0	Sets Carrier Detect Mode vs. Low Battery Mode

Table 13. Control Bit Listing (By Function) (continued)

Power Down Control

Register	Bit No.	Power Up Default	**Function** (when bit = 1 if appropriate)
5	0	0	Power down the Reference Oscillator
5	1	0	Power down the T_X PLL.
5	2	0	Power down the R_X PLL.
5	3	0	Power down the LO2 PLL.
5	4	0	Power down the R_X Data Path. Includes Data Slicer, Clock Recovery, Descrambler, Data Detect, and Status circuits.
5	5	0	Power down the CVSD Decoder.
5	6	0	Power down the R_X Audio path (Pin 32 to 30). Includes AALPF, LPF, and Gain Adjust circuits.
5	7	0	Power down the Power Amplifiers (Pins 27, 28)
5	8	0	Power down the T_X Audio Path (Pin 25 to 22). Includes micro–phone amplifier, LPF, and Smoothing LPF circuits.
5	9	0	Power down the CVSD Encoder, Idle Channel Detector, 1010 Generator, T_X Data Register, and Scrambler circuits.
5	10	0	Power down the Low Battery/Carrier Detect Circuit.
5	18	0	Power down the Idle Channel Detection Circuit.

Table 14. Register Map

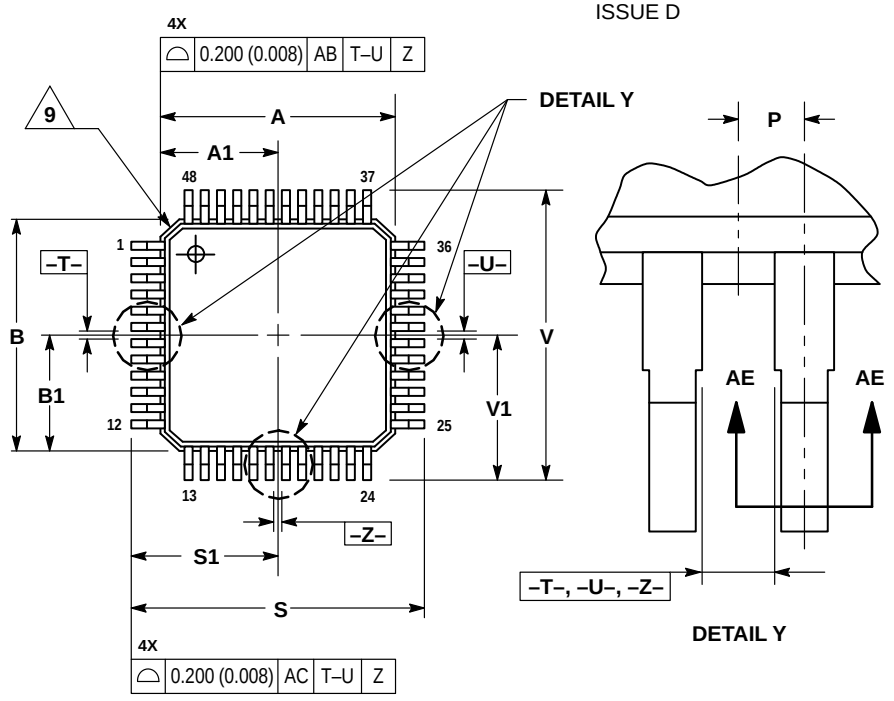
Register Address	Register Number	MSB 23	22	21	20	19	18	17	16	15	14	13	12
0001	1		CVSD Decoder Minimum Step Size		Tx PhDet. Curr. Sel.	13 Bit Tx N Counter Divide Value (Bits 19 – 7)							
0010	2		CVSD Encoder Minimum Step Size		Rx PhDet. Curr. Sel.	13 Bit Rx N' Counter Divide Value (Bits 19 – 7)							
0011	3	Sets Low Battery/Carrier Detect Threshold			Adjust VB Reference Voltage				Set CVSD for the selected Clock Rate		LO2 PhD Curr. Sel.	14 bit LO2 Counter Divide Value (Bits 13 – 0)	
0100	4	6 Bit Encode Clock Counter Divide Value						6 Bit Switched Capacitor Filter Counter Divide Value					
0101	5	LB/CD Det. Out	Status Output	Idle Chan. Output	Data Modem Mode	Invert Data Slicer	Idle Channel Disable	Sets Idle Channel Threshold Level			4 Bit Idle Channel Counter Delay Value (Bits 14 – 11)		
0110	6									Remote Gain Adjust (Bits 15 – 11)			
0111	7	Tx Phase Detector Polarity	Rx Phase Detector Polarity	LO2 Ph. Detector Polarity	LO2 Capacitor Select			Production Test Modes & Data Modem Mode			Idle Charge Disable	FTxMC/ FRxMC Level	Data Word Size (16/24 bit)
1000	8	16 or 24 Bit Code Word for the Tx Data Register (Bits 23 – 0)											
1001	9	16 or 24 Bit Data Word for the Tx Data Register (Bits 23 – 0)											
1010	10	16 or 24 Bit Data Word Output from the Rx Data Register (Bits 23 – 0)											

Register Address	Register Number	11	10	9	8	7	6	5	4	3	2	1	LSB 0
0001	1	13 Bit Tx N Counter Divide Value (Bits 19 – 7)					7 Bit Tx A Counter Divide Value						
0010	2	13 Bit Rx N' Counter Divide Value (Bits 19 – 7)					7 Bit Rx A' Counter Divide Value						
0011	3	14 bit LO2 Counter Divide Value (Bits 13 – 0)											
0100	4	12 Bit Reference Counter Divide Value											
0101	5	4 Bit Idle Channel Ctr. Value	LB/CD Detect Disable	CVSD Encoder Disable	Tx Audio Path Disable	Power Amplifier Disable	Rx Audio Path Disable	CVSD Decoder Disable	Rx Data Path Disable	LO2 PLL Disable	Rx PLL Disable	Tx PLL Disable	Ref. Osc. Disable
0110	6	Remote Gain Adj.	Rx Audio Path Gain Adjust (28.5 dB range)					Set CD Mode	Tx 1010 Generator	Rx 1010 Generator	Mute Tx Audio	Mute Rx Audio	Mute Pwr. Amps
0111	7	Code Word Size (16/24 bit)	Scrambler/Descrambler Tap Selection			MP2 Mode (See Table 7)		MP1 Mode (See Table 6)		Bypass Data Detect	Disable Idle Chnl. Detection	Bypass Scrambler/ Descrambler	Bypass Clock Recovery
1000	8	16 or 24 Bit Code Word for the Tx Data Register (Bits 23 – 0)											
1001	9	16 or 24 Bit Data Word for the Tx Data Register (Bits 23 – 0)											
1010	10	16 or 24 Bit Data Word Output from the Rx Data Register (Bits 23 – 0)											

Note: Shaded areas represent output bits to be read out.

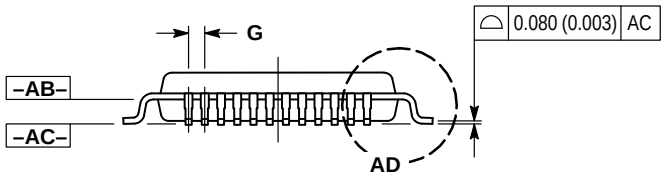
OUTLINE DIMENSIONS

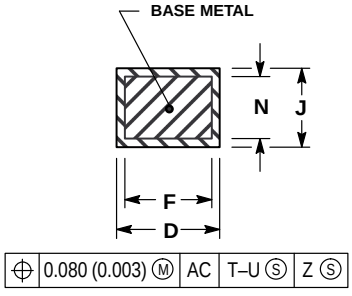
FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(LQFP–48)
ISSUE D



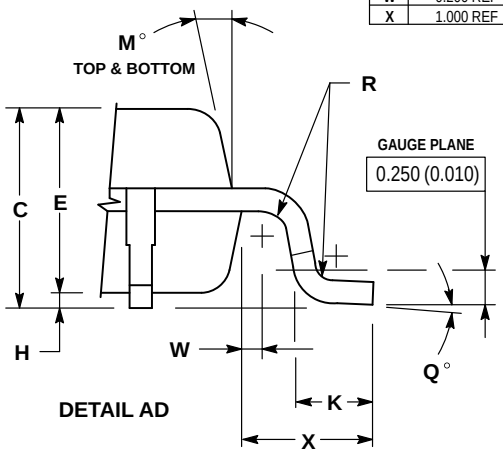
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BASIC		0.020 BASIC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12 °REF		12 °REF	
N	0.090	0.160	0.004	0.006
P	0.250 BASIC		0.010 BASIC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	





SECTION AE–AE



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